UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/000,087	12/04/2001	Tetsuya Shimizu	35.C16002	8033

5514 7590 04/20/2007

FITZPATRICK CELLA HARPER & SCINTO
30 ROCKEFELLER PLAZA
NEW YORK, NY 10112

EXAMINER	
GILES, NICHOLAS G	
ART UNIT	PAPER NUMBER
2622	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	04/20/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/000,087	SHIMIZU, TETSUYA	
	Examiner	Art Unit	
	Nicholas G. Giles	2622	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 February 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3,4 and 6-10* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3,4 and 6-10* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *24 December 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 01/08/2007 has been entered.

Response to Arguments

2. Applicant's arguments filed 01/08/2007 have been fully considered but they are not persuasive. Applicant argues that the SDRAM in Okada is relied upon in the rejection. The examiner points out that in section 3 of Okada the memories are built on the same IC. Applicant further argues that Tojo doesn't teach moving and still capture. The examiner points out that Tojo was not relied upon to show moving and still capture, but instead was used to show that the second memory is removable.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims **1, 3-4, and 6-7** are rejected under 35 U.S.C. 103(a) as being unpatentable over Juen (U.S. Pub. No. 2002/0024602) in view of Okada et al. (Article: System on a Chip for Digital Still Camera) in further view of Tojo et al. (U.S. Patent No. 5,737,014).

Regarding claim **1**, Juen discloses:

> An image pickup apparatus comprising: image pickup means for outputting an image signal having a first number of pixels which is greater than a predetermined number of pixels (imaging means 1 Fig. 1 and ¶0040); converting means for converting a moving image signal having the first number of pixels, outputted from said image pickup means, into an image signal having the predetermined number of pixels (pixel density conversion means 2 Fig. 1 and ¶0040); a first memory having storage capacity corresponding to the predetermined number of pixels, for storing the moving image signal having the predetermined number of pixels, outputted from said converting means (moving image recording means 3 Fig. 1 which includes coding conversion circuit 21 which includes memory 42, ¶0079, ¶0070, and ¶0073); a second memory having storage capacity corresponding to the first number of pixels (buffer 5 Fig. 2 which includes memory 22, ¶0079); and a memory interface arranged to generate addresses of said second memory, to write into said second memory a still image signal of the first number of pixels outputted from said image pickup

means, and to read out a still image signal of the first number of pixels from said second memory (¶0043); still image processing means for processing the still image signal having the first number of pixels, read out by said memory interface (¶0043); and recording means for recording the moving image signal read out from said first memory on a recording medium in accordance with a predetermined recording format (¶0038-0039), wherein the predetermined number of pixels conforms to the predetermined recording format (¶0090)

Juen is silent with regards combining components onto the same integrated circuit. Okada et al. discloses:

Converting means, said first memory, said memory interface, and said still image processing means are provided on a single integrated circuit, said image pickup means is built as a circuit difference from said single integrated circuit (see section 3 and Fig. 1).

An advantage to combining components onto the same integrated circuit is that the camera can realize pocket-sized, high-speed, low-power, video clip, sequential shot and various functions as Okada et al. discloses in the abstract.

Juen and Okada are silent with regards to the second memory being a separate integrated circuit and the memory interface being capable of generating addresses of a memory of larger capacity than the second memory. Tojo et al. discloses using removable buffer memory who's size can be increased, which would be a separate circuit than the integrated circuit and where the memory interface is capable of

generating addresses of a memory of larger capacity than the second memory, as a buffer memory in a camera (memory 7 Fig. 1, 2:67-3:9, 3:65-4:2, and 5:56-60). Juen's camera uses buffer memory and therefore the removable buffer memory of Tojo et al. could be used in its place. An advantage to making the second memory on a separate circuit and the memory interface being capable of generating addresses of a memory of larger capacity than the second memory is that as memory sizes get larger they can be used as replacements in the removable buffer memory setup as can be seen in Tojo in 5:56-60. For this reason it would have been obvious to one of ordinary skill in the art at the time the invention was made to have Juen's camera include the first memory and still image processing means on one integrated circuit and the second memory on a separate circuit where the memory interface is capable of generating addresses of a memory of larger capacity than the second memory.

Regarding claim **3**, see the rejection of claim 1 and note that Juen further discloses:

> Special effect means for performing a special effect processing on the image signal having the predetermined number of pixels, stored in said first memory and outputting the thus-processed image signal (¶0070-¶0078 done through Coding conversion component 21 included in moving image recording means 3 Fig. 1).

Note that the limitation of providing components (in this case the special effect means) on the same integrated circuit was covered in the rejection of claim 1.

Regarding claim **4**, see the rejection of claim 1 and note that Juen further discloses:

> Output means for converting the image signal having the predetermined number of pixels, stored in said first memory into a predetermined format and outputting the thus-converted image signal (encoding conversion component 6 Fig. 3, ¶0047 and ¶0090).

Note that the limitation of providing components (in this case the output means) on the same integrated circuit was covered in the rejection of claim 1.

Regarding claim **6**, see the rejection of claim 1 and note that Juen further discloses:

> Still image processing means includes encoding means for encoding the image signal outputted from said second memory and compressing an amount of information of the image signal (coding conversion component 21 included in compression means 7 Fig. 5, ¶0070-0078, ¶0049, ¶0090, and ¶0108).

Regarding claim **7**, see the rejection of claim 1 and note that Juen further discloses reducing the pixel resolution to ½ of the original resolution in moving image mode (¶0058 and ¶0084) and leaving the resolution as is in still image mode. (¶0052, note there is no pixel density conversion means between the imaging means 1 and the still image recording means 4) Juen is silent with regards to adding signals of pixels of vertically adjacent lines of the image pickup elements for the moving image. Okada et al. discloses adding vertically adjacent lines of the image pickup elements for a moving

image (¶0032-0034 and 0056). An advantage to adding vertically adjacent lines of the image pickup elements for a moving image is that finer processing of image can be performed as Okada et al. discloses in ¶0019. For this reason it would have been obvious to one of ordinary skill in the art at the time the invention was made to have Juen device include adding vertically-adjacent lines of the image pickup elements for a moving image.

4. Claims **8-9** are rejected under 35 U.S.C. 103(a) as being unpatentable over Juen in view of Okada et al. in further view of Tojo et al. in further view of Motono (U.S. Patent No. 6,603,866).

Regarding claim **8**, see the rejection of claim 1 and note that Juen further discloses:

> Moving image processing means for reading out from said first memory an image signal having the predetermined number of pixels and outputting the read-out image signal as moving image data (¶0039); first recording means for recording to a first recording medium the moving image data outputted form said moving image processing means (¶0039); and second recording means for recording to a second recording medium, the still image data outputted from said still image processing means (¶0039 and ¶0114).

Juen, Okada, and Tojo are silent with regards to storing the moving image data and still image data on different recording mediums. Motono et al. discloses storing

moving and still images on different materials in 2:56-3:2 and 3:51-59. An advantage to storing the data on different mediums is that the user has quick access to the type of imaging desired and doesn't have to spend time sorting through one medium. For this reason it would have been obvious to one of ordinary skill in the art at the time the invention was made to have Juen's camera include storing the still images and moving images on different recording mediums.

Regarding claim **9**, see the rejection of claim 8 and note that Juen further discloses that the recording mediums can be magnetic tape and a memory card (¶0114).

5. Claim **10** is rejected under 35 U.S.C. 103(a) as being unpatentable over Juen (U.S. Pub. No. 2002/0024602) in view of Wilder et al. (U.S. Patent no. 5,262,871) in further view of Okada et al. (Article: System on a Chip for Digital Still Camera) in further view of Tojo et al. (U.S. Patent No. 5,737,014).

Regarding claim **10**, Juen discloses:

> An image processing apparatus comprising: an input unit arranged to input an image signal having a first number of pixels which is greater than a predetermined number of pixels; a conversion circuit arranged to convert a moving image signal having the first number of pixels into an image signal having the predetermined number of pixels (pixel density conversion means 2 Fig. 1 and ¶0040); a first memory having storage capacity sufficient for the predetermined number of pixels, arranged to

store the moving image signal having the predetermined number of pixels, outputted from said conversion circuit (moving image recording means 3 Fig. 1 which includes coding conversion circuit 21 which includes memory 42, ¶0079, ¶0070, and ¶0073); a second memory having a storage capacity corresponding to the first number of pixels (buffer 5 Fig. 2 which includes memory 22, ¶0079); and a memory interface arranged to write into said second memory a still image signal having the first number of pixels (¶0043); a still image processing circuit arranged to process the still image signal having the first number of pixels, read out by said memory interface (¶0043); and a record unit arranged to record the moving image signal read out from said first memory on a recording medium in accordance with a predetermined recording format (¶0038-0039), wherein the predetermined number of pixels conforms to the predetermined recording format (¶0090).

Juen is silent with regards to the input unit being capable of inputting image signals of different numbers of pixels. Wilder et al. discloses this in 5:17-23. An advantage to inputting images at different numbers of pixels is lower number of pixel images can be rapidly scanned for regions of interest before capturing the image with a higher number of pixels. For this reason it would have been obvious to one of ordinary skill in the art at the time the invention was made to have Juen apparatus include the input unit being capable of inputting image signals of different numbers of pixels.

Juen and Wilder are silent with regards combining components onto the same integrated circuit. Okada et al. discloses:

> Converting circuit, said first memory, said memory interface, and said still image processing circuit are provided on a single integrated circuit (see section 3 and Fig. 1).

An advantage to combining components onto the same integrated circuit is that the camera can realize pocket-sized, high-speed, low-power, video clip, sequential shot and various functions as Okada et al. discloses in the abstract.

Juen, Wilder, and Okada are silent with regards to the second memory being a separate integrated circuit and the memory interface being capable of generating addresses of a memory of larger capacity than the second memory. Tojo et al. discloses using removable buffer memory who's size can be increased, which would be a separate circuit than the integrated circuit and where the memory interface is capable of generating addresses of a memory of larger capacity than the second memory, as a buffer memory in a camera (memory 7 Fig. 1, 2:67-3:9, 3:65-4:2, and 5:56-60). Juen's camera uses buffer memory and therefore the removable buffer memory of Tojo et al. could be used in its place. An advantage to making the second memory on a separate circuit and the memory interface being capable of generating addresses of a memory of larger capacity than the second memory is that as memory sizes get larger they can be used as replacements in the removable buffer memory setup as can be seen in Tojo in 5:56-60. For this reason it would have been obvious to one of ordinary skill in the art at the time the invention was made to have Juen's camera include the converting circuit,

first memory, and still image processing circuit on one integrated circuit and the second memory on a separate circuit where the memory interface is capable of generating addresses of a memory of larger capacity than the second memory.

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nicholas G. Giles whose telephone number is (571) 272-2824. The examiner can normally be reached on Monday through Friday from 7:30am to 4:00pm EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ngoc - Yen Vu can be reached on (571) 272-7320. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

NGG

NGOC-YEN VU
SUPERVISORY PATENT EXAMINER